CMOS Latched 8-/16-Channel Analog Multiplexers

ADG526A/ADG527A

FEATURES

44 V supply maximum rating
V_{SS} to V_{DD} analog signal range
Single- or dual-supply specifications
Wide supply ranges (10.8 V to 16.5 V)
Microprocessor compatible (100 ns $\overline{WR}$ pulse)
Extended plastic temperature range (−40°C to +85°C)
Low leakage (20 pA typical)
Low power dissipation (28 mW maximum)
Available in PDIP, CERDIP, SOIC, and PLCC packages
Superior alternative to DG526 and DG527

APPLICATIONS

Data acquisition systems
Communication systems
Automatic test equipment
Microprocessor controlled systems

GENERAL DESCRIPTION

The ADG526A and ADG527A are CMOS monolithic analog multiplexers with 16 single channels and dual 8 channels, respectively. On-chip latches facilitate microprocessor interfacing.

The ADG526A switches one of 16 inputs to a common output, depending on the state of four binary addresses and an enable input. The ADG527A switches one of eight differential inputs to a common differential output, depending on the state of three binary addresses and an enable input. Both devices have TTL and 5 V CMOS logic-compatible digital inputs.

The ADG526A and ADG527A are designed on an enhanced LC²MOS process that gives an increased signal capability of V_{SS} to V_{DD} and enables operation over a wide range of supply voltages. The devices can comfortably operate anywhere in the 10.8 V to 16.5 V single- or dual-supply range. These multiplexers also feature high switching speeds and low R_{ON}.

FUNCTIONAL BLOCK DIAGRAMS

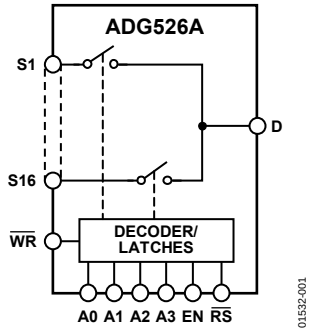

Figure 1. ADG526A

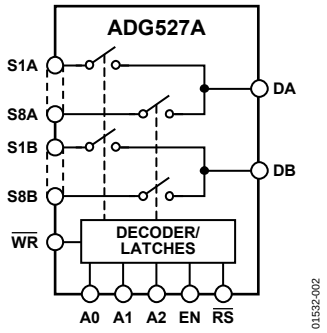

Figure 2. ADG527A

PRODUCT HIGHLIGHTS

1. Single- or Dual-Supply Specifications with a Wide Tolerance. The devices are specified in the 10.8 V to 16.5 V range for both single and dual supplies.
2. Easily Interfaced. The ADG526A and ADG527A can be easily interfaced with microprocessors. The $\overline{WR}$ signal latches the state of the address control lines and the enable line. The $\overline{RS}$ signal clears both the address and enable data in the latches, resulting in no output (all switches off). $\overline{RS}$ can be tied to the microprocessor reset pin.
3. Extended Signal Range. The enhanced LC²MOS processing results in a high breakdown and an increased analog signal range from V_{SS} to V_{DD}.
4. Break-Before-Make Switching. Switches are guaranteed break-before-make so that input signals are protected against momentary shorting.
5. Low Leakage. Leakage currents in the range of 20 pA make these multiplexers suitable for high precision circuits.

Rev. C

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SPECIFICATIONS

DUAL SUPPLY

V_{DD} = 10.8 V to 16.5 V, V_{SS} = −10.8 V to −16.5 V, unless otherwise noted.

Table 1.

	ADG526A/ADG527A				ADG526A			
	K Version		B Version		T Version			
Parameter	**25°C**	**−40°C to +85°C**	**25°C**	**−40°C to +85°C**	**25°C**	**−55°C to +125°C**	**Unit**	**Comments**
ANALOG SWITCH								
Analog Signal Range	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V min	
	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V max	
R_{ON}	280		280		280		Ω typ	−10 V ≤ V_S ≤ +10 V, I_{DS} = 1 mA; see Figure 15
	450	600	450	600	450	600	Ω max	
	300	400	300	400			Ω max	V_{DD} = +15 V (±10%), V_{SS} = −15 V (±10%)
					300	400	Ω max	V_{DD} = +15 V (±5%), V_{SS} = −15 V (±5%)
R_{ON} Drift	0.6		0.6		0.6		%/°C typ	−10 V ≤ V_S ≤ +10 V, I_{DS} = 1 mA
R_{ON} Match	5		5		5		% typ	−10 V ≤ V_S ≤ +10 V, I_{DS} = 1 mA
I_S (Off), Off Input Leakage	0.02		0.02		0.02		nA typ	V1 = ±10 V, V2 = ∓10 V; see Figure 16
	1	50	1	50	1	50	nA max	
I_D (Off), Off Output Leakage	0.04		0.04		0.04		nA typ	V1 = ±10 V, V2 = ∓10 V; see Figure 17
ADG526A	1	200	1	200	1	200	nA max	
ADG527A	1	100	1	100			nA max	
I_D (On), On Channel Leakage	0.04		0.04		0.04		nA typ	V1 = ±10 V, V2 = ∓10 V; see Figure 18
ADG526A	1	200	1	200	1	200	nA max	
ADG527A	1	100	1	100			nA max	
I_{DIFF}, Differential Off Output Leakage (ADG527A Only)		25		25			nA max	V1 = ±10 V, V2 = ∓10 V; see Figure 19
DIGITAL CONTROL								
V_{INH}, Input High Voltage		2.4		2.4		2.4	V min	
V_{INL}, Input Low Voltage		0.8		0.8		0.8	V max	
I_{INL} or I_{INH}		1		1		1	μA max	V_{IN} = 0 to V_{DD}
C_{IN}, Digital Input Capacitance	8		8		8		pF max	
DYNAMIC CHARACTERISTICS[1]								
$t_{TRANSITION}$	200		200		200		ns typ	V1 = ±10 V, V2 = ∓10 V; see Figure 20
	300	400	300	400	300	400	ns max	
t_{OPEN}	50		50		50		ns typ	See Figure 21
	25	10	25	10	25	10	ns min	
t_{ON} (EN, $\overline{WR}$)	200		200		200		ns typ	See Figure 22 and Figure 23
	300	400	300	400	300	400	ns max	
t_{OFF} (EN, $\overline{RS}$)	200		200		200		ns typ	See Figure 22 and Figure 24
	300	400	300	400	300	400	ns max	
t_W , Write Pulse Width	100	120	100	120	100	130	ns min	See Figure 13
t_S, Address Enable Setup Time		100		100		100	ns min	See Figure 13
t_H, Address Enable Hold Time		10		10		10	ns min	See Figure 13
t_{RS}, Reset Pulse Width		100		100		100	ns min	See Figure 14

Parameter	ADG526A/ADG527A K Version 25°C	ADG526A/ADG527A K Version −40°C to +85°C	ADG526A/ADG527A B Version 25°C	ADG526A/ADG527A B Version −40°C to +85°C	ADG526A T Version 25°C	ADG526A T Version −55°C to +125°C	Unit	Comments
Off Isolation	68		68		68		dB typ	V_{EN} = 0.8 V, R_L = 1 kΩ, C_L = 15 pF, V_S = 7 V rms, f = 100 kHz
	50		50		50		dB min	V_S = 7 V rms, f = 100 kHz
C_S (Off)	5		5		5		pF typ	V_{EN} = 0.8 V
C_D (Off)								
ADG526A	44		44		44		pF typ	V_{EN} = 0.8 V
ADG527A	22		22				pF typ	
Q_{INJ}, Charge Injection	4		4		4		pC typ	R_S = 0 Ω, V_S = 0 V; see Figure 25
POWER SUPPLY								
I_{DD}	0.6		0.6		0.6		mA typ	V_{IN} = V_{INL} or V_{INH}
		1.5		1.5		1.5	mA max	
I_{SS}	20		20		20		µA typ	V_{IN} = V_{INL} or V_{INH}
		0.2		0.2		0.2	mA max	
Power Dissipation	10		10		10		mW typ	
		28		28		28	mW max	

[1] Sample tested at 25°C to ensure compliance.

SINGLE SUPPLY

V_{DD} = 10.8 V to 16.5 V, V_{SS} = GND to 0 V, unless otherwise noted.

Table 2.

	ADG526A/ADG527A				ADG526A			
	K Version		B Version		T Version			
Parameter	**25°C**	**−40°C to +85°C**	**25°C**	**−40°C to +85°C**	**25°C**	**−55°C to +125°C**	**Unit**	**Comments**
ANALOG SWITCH								
Analog Signal Range	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V min	
	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V max	
R_{ON}	500		500		500		Ω typ	0 V ≤ V_S ≤ 10 V, I_{DS} = 0.5 mA; see Figure 15
	700	1000	700	1000	700	1000	Ω max	
R_{ON} Drift	0.6		0.6		0.6		%/°C typ	0 V ≤ V_S ≤ 10 V, I_{DS} = 0.5 mA
R_{ON} Match	5		5		5		% typ	0 V ≤ V_S ≤ 10 V, I_{DS} = 0.5 mA
I_S (Off), Off Input Leakage	0.02		0.02		0.02		nA typ	V1 = 10 V/0 V, V2 = 0 V/10 V; see Figure 16
	1	50	1	50	1	50	nA max	
I_D (Off), Off Output Leakage	0.04		0.04		0.04		nA typ	V1 = 10 V/0 V, V2 = 0 V/10 V; see Figure 17
ADG526A	1	200	1	200	1	200	nA max	
ADG527A	1	100	1	100			nA max	
I_D (On), On Channel Leakage	0.04		0.04		0.04		nA typ	V1 = 10 V/0 V, V2 = 0 V/10 V; see Figure 18
ADG526A	1	200	1	200	1	200	nA max	
ADG527A	1	100	1	100			nA max	
I_{DIFF}, Differential Off Output Leakage (ADG527A Only)		25		25			nA max	V1 = 10 V/0 V, V2 = 0 V/10 V; see Figure 19
DIGITAL CONTROL								
V_{INH}, Input High Voltage		2.4		2.4		2.4	V min	
V_{INL}, Input Low Voltage		0.8		0.8		0.8	V max	
I_{INL} or I_{INH}		1		1		1	μA max	V_{IN} = 0 to V_{DD}
C_{IN}, Digital Input Capacitance	8		8		8		pF max	
DYNAMIC CHARACTERISTICS[1]								
$t_{TRANSITION}$	300		300		300		ns typ	V1 = 10 V/0 V, V2 = 0 V/10 V; see Figure 20
	450	600	450	600	450	600	ns max	
t_{OPEN}	50		50		50		ns typ	See Figure 21
	25	10	25	10	25	10	ns min	
t_{ON} (EN, $\overline{WR}$)	250		250		250		ns typ	See Figure 22 and Figure 23
	450	600	450	600	450	600	ns max	
t_{OFF} (EN, $\overline{RS}$)	250		250		250		ns typ	See Figure 22 and Figure 24
	450	600	450	600	450	600	ns max	
t_W Write Pulse Width	100	120	100	120	100	130	ns min	See Figure 13
t_S Address Enable Setup Time		100		100		100	ns min	See Figure 13
t_H Address Enable Hold Time		10		10		10	ns min	See Figure 13
t_{RS} Reset Pulse Width		100		100		100	ns min	See Figure 14
Off Isolation	68		68		68		dB typ	V_{EN} = 0.8 V, R_L = 1 kΩ, C_L = 15 pF
	50		50		50		dB min	V_S = 3.5 V rms, f = 100 kHz

Parameter	ADG526A/ADG527A K Version 25°C	ADG526A/ADG527A K Version −40°C to +85°C	ADG526A/ADG527A B Version 25°C	ADG526A/ADG527A B Version −40°C to +85°C	ADG526A T Version 25°C	ADG526A T Version −55°C to +125°C	Unit	Comments
C_S (Off)	5		5		5		pF typ	V_{EN} = 0.8 V
C_D (Off)								
ADG526A	44		44		44		pF typ	V_{EN} = 0.8 V
ADG527A	22		22				pF typ	
Q_{INJ}, Charge Injection	4		4		4		pC typ	R_S = 0 Ω, V_S = 0 V; see Figure 25
POWER SUPPLY								
I_{DD}	0.6		0.6		0.6		mA typ	V_{IN} = V_{INL} or V_{INH}
		1.5		1.5		1.5	mA max	
Power Dissipation	11		11		11		mW typ	
		25		25		25	mW max	

[1] Sample tested at 25°C to ensure compliance.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to V_{SS}	44 V
V_{DD} to GND	25 V
V_{SS} to GND	−25 V
Analog Inputs[1]	
Voltage at Sx or Dx Pins	V_{SS} − 2 V to V_{DD} + 2 V or 20 mA, whichever occurs first
Continuous Current, Sx or Dx Pins	20 mA
Pulsed Current, Sx or Dx Pins	
1 ms Duration, 10% Duty Cycle	40 mA
Digital Inputs[1]	
Voltage at A, EN, $\overline{WR}$, $\overline{RS}$	V_{SS} − 4 V to V_{DD} + 4 V or 20 mA, whichever occurs first
Power Dissipation (Any Package)	
Up to 75°C	470 mW
Derates Above 75°C	6 mW/°C
Operating Temperature Range	
Commercial (K Version)	−40°C to +85°C
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

[1] Overvoltage at A, EN, $\overline{WR}$, $\overline{RS}$, Sx, or Dx pins are clamped by diodes. Limit current to the maximum rating in Table 3.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

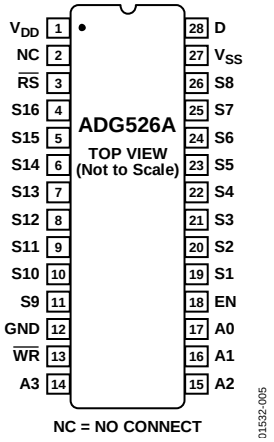


Figure 3. ADG526A PDIP, SOIC, and CERDIP Pin Configuration

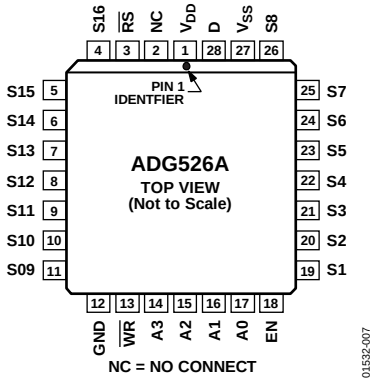


Figure 4. ADG526A PLCC Pin Configuration

Table 4. ADG526A Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD}	Most Positive Power Supply Potential.
2	NC	No Connect.
3	$\overline{RS}$	Reset. The $\overline{RS}$ signal clears both the address and enable data in the latches resulting in no output (all switches off).
4	S16	Source Terminal. This pin can be an input or output.
5	S15	Source Terminal. This pin can be an input or output.
6	S14	Source Terminal. This pin can be an input or output.
7	S13	Source Terminal. This pin can be an input or output.
8	S12	Source Terminal. This pin can be an input or output.
9	S11	Source Terminal. This pin can be an input or output.
10	S10	Source Terminal. This pin can be an input or output.
11	S9	Source Terminal. This pin can be an input or output.
12	GND	Ground (0 V) Reference.
13	$\overline{WR}$	Write. The $\overline{WR}$ signal latches the state of the address control lines and the enable line.
14	A3	Logic Control Inputs. Selects which source terminal is connected to the drain (D).
15	A2	Logic Control Inputs. Selects which source terminal is connected to the drain (D).
16	A1	Logic Control Inputs. Selects which source terminal is connected to the drain (D).
17	A0	Logic control inputs. Selects which source terminal is connected to the drain (D).
18	EN	Enable. Active high logic control input.
19	S1	Source Terminal. This pin can be an input or output.
20	S2	Source Terminal. This pin can be an input or output.
21	S3	Source Terminal. This pin can be an input or output.
22	S4	Source Terminal. This pin can be an input or output.
23	S5	Source Terminal. This pin can be an input or output.
24	S6	Source Terminal. This pin can be an input or output.
25	S7	Source Terminal. This pin can be an input or output.
26	S8	Source Terminal. This pin can be an input or output.
27	V_{SS}	Most Negative Power Supply Potential.
28	D	Drain Terminal. This pin can be an input or output.

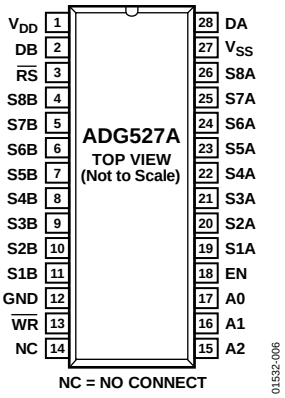


Figure 5. ADG527A PDIP, SOIC Pin Configuration

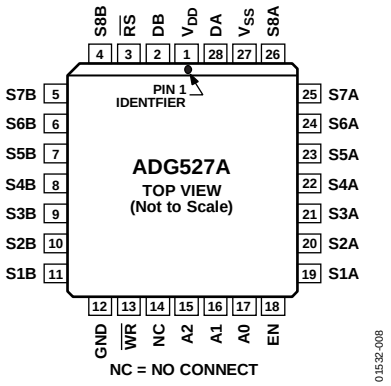


Figure 6. ADG527A PLCC Pin Configuration

Table 5. ADG527A Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD}	Most Positive Power Supply Potential.
2	DB	Drain Terminal. This pin can be an input or output.
3	$\overline{RS}$	Reset. The $\overline{RS}$ signal clears both the address and enable data in the latches resulting in no output (all switches off).
4	S8B	Source Terminal. This pin can be an input or output.
5	S7B	Source Terminal. This pin can be an input or output.
6	S6B	Source Terminal. This pin can be an input or output.
7	S5B	Source Terminal. This pin can be an input or output.
8	S4B	Source Terminal. This pin can be an input or output.
9	S3B	Source Terminal. This pin can be an input or output.
10	S2B	Source Terminal. This pin can be an input or output.
11	S1B	Source Terminal. This pin can be an input or output.
12	GND	Ground (0 V) Reference.
13	$\overline{WR}$	Write. The $\overline{WR}$ signal latches the state of the address control lines and the enable line.
14	NC	No Connect.
15	A2	Logic Control Inputs. Selects which source terminal is connected to the drain (D).
16	A1	Logic Control Inputs. Selects which source terminal is connected to the drain (D).
17	A0	Logic Control Inputs. Selects which source terminal is connected to the drain (D).
18	EN	Enable. Active high logic control input.
19	S1A	Source Terminal. This pin can be an input or output.
20	S2A	Source Terminal. This pin can be an input or output.
21	S3A	Source Terminal. This pin can be an input or output.
22	S4A	Source Terminal. This pin can be an input or output.
23	S5A	Source Terminal. This pin can be an input or output.
24	S6A	Source Terminal. This pin can be an input or output.
25	S7A	Source Terminal. This pin can be an input or output.
26	S8A	Source Terminal. This pin can be an input or output.
27	V_{SS}	Most Negative Power Supply Potential.
28	DA	Drain Terminal. This pin can be an input or output.

Table 6. ADG526A Truth Table[1]

A3	A2	A1	A0	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH
X	X	X	X	X	↓	1	Retains previous switch condition
X	X	X	X	X	X	0	None (address and enable latches cleared)
X	X	X	X	0	0	1	None
0	0	0	0	1	0	1	1
0	0	0	1	1	0	1	2
0	0	1	0	1	0	1	3
0	0	1	1	1	0	1	4
0	1	0	0	1	0	1	5
0	1	0	1	1	0	1	6
0	1	1	0	1	0	1	7
0	1	1	1	1	0	1	8
1	0	0	0	1	0	1	9
1	0	0	1	1	0	1	10
1	0	1	0	1	0	1	11
1	0	1	1	1	0	1	12
1	1	0	0	1	0	1	13
1	1	0	1	1	0	1	14
1	1	1	0	1	0	1	15
1	1	1	1	1	0	1	16

[1] X = don't care.

Table 7. ADG527A Truth Table[1]

A2	A1	A0	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH PAIR
X	X	X	X	↓	1	Retains previous switch condition
X	X	X	X	X	0	None (address and enable latches cleared)
X	X	X	0	0	1	None
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

[1] X = don't care.

TYPICAL PERFORMANCE CHARACTERISTICS

The multiplexers are guaranteed functional with reduced single or dual supplies down to 4.5 V.

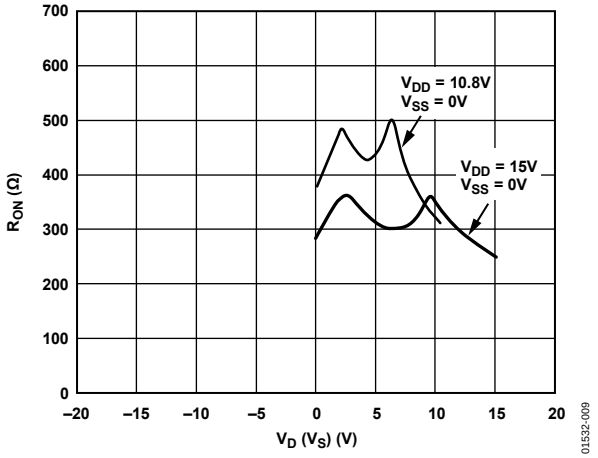


Figure 7. R_{ON} as a Function of V_D (V_S): Single-Supply Voltage, T_A = 25°C

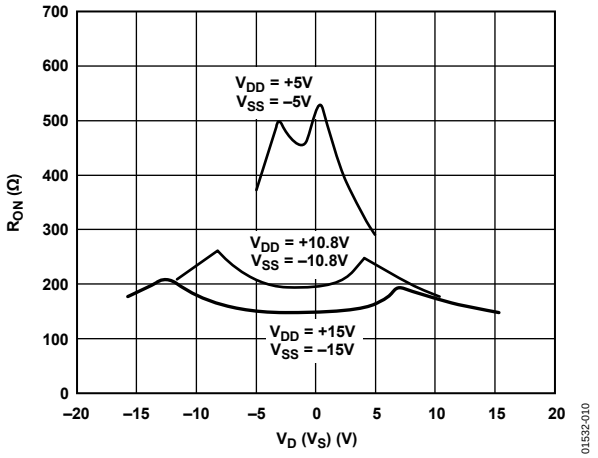


Figure 8. R_{ON} as a Function of V_D (V_S): Dual-Supply Voltage, T_A = 25°C

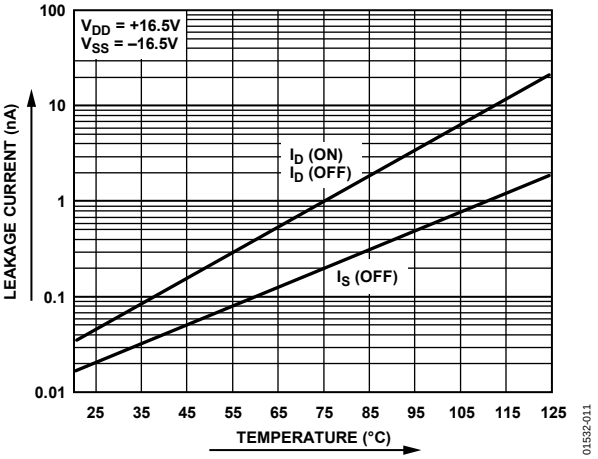


Figure 9. Leakage Current as a Function of Temperature (Leakage Currents Reduce as the Supply Voltages Reduce)

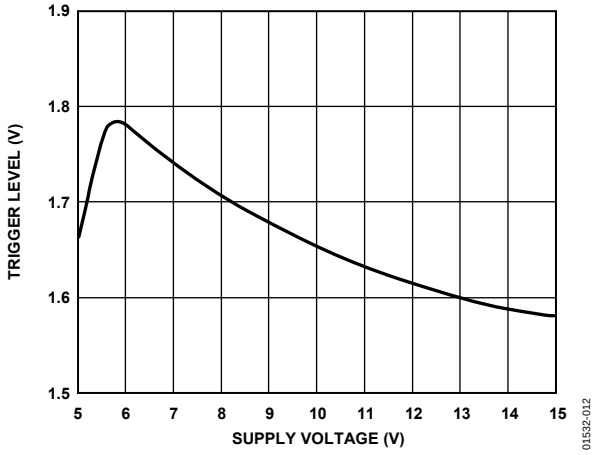


Figure 10. Trigger Levels vs. Power Supply Voltage, Dual or Single Supply, T_A = 25°C

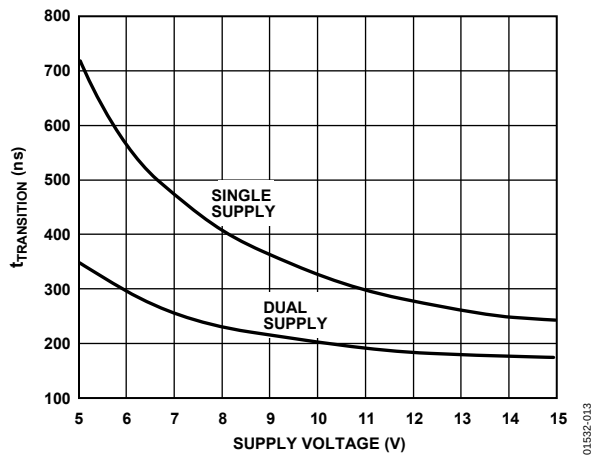


Figure 11. $t_{TRANSITION}$ vs. Supply Voltage: Dual and Single Supplies, T_A = 25°C (Note: For V_{DD} and V_{SS} <10 V; V1 = V_{DD}/V_{SS}, V2 = V_{SS}/V_{DD}; See Figure 20)

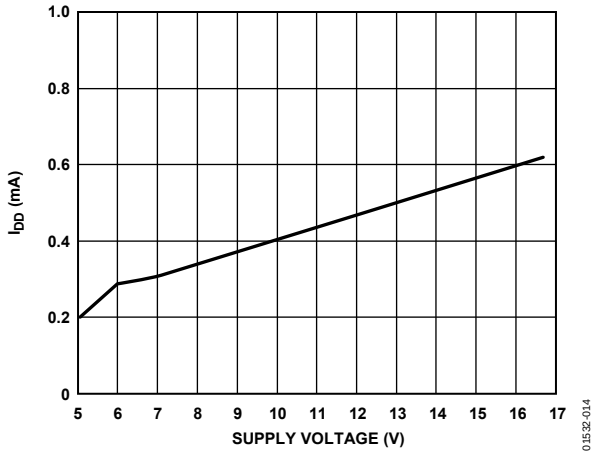


Figure 12. I_{DD} vs. Supply Voltage: Dual or Single Supply, T_A = 25°C

TERMINOLOGY

R_{ON}
Ohmic resistance between Terminal D and Terminal S.

R_{ON} Match
Difference between the R_{ON} of any two channels.

R_{ON} Drift
Change in R_{ON} vs. temperature.

I_S (Off)
Source terminal leakage current when the switch is off.

I_D (Off)
Drain terminal leakage current when the switch is off.

I_D (On)
Leakage current that flows from the closed switch into the body.

V_S (V_D)
Analog voltage on Terminal S or Terminal D.

C_S (Off)
Channel input capacitance for off condition.

C_D (Off)
Channel output capacitance for off condition.

C_{IN}
Digital input capacitance.

t_{ON} (EN)
Delay time between the 50% and 90% points of the digital input and switch on condition.

t_{OFF} (EN)
Delay time between the 50% and 10% points of the digital input and switch off condition.

$t_{TRANSITION}$
Delay time between the 50% and 90% points of the digital inputs and switch on condition when switching from one address state to another.

t_{OPEN}
Off time measured between 50% points of both switches when switching from one address state to another.

V_{INL}
Maximum input voltage for Logic 0.

V_{INH}
Minimum input voltage for Logic 1.

I_{INL} (I_{INH})
Input current of the digital input.

V_{DD}
Most positive voltage supply.

V_{SS}
Most negative voltage supply.

I_{DD}
Positive supply current.

I_{SS}
Negative supply current.

TIMING

Figure 13 shows the timing sequence for latching the switch address and enable inputs. The latches are level sensitive; therefore, while $\overline{WR}$ is held low, the latches are transparent and the switches respond to the address and enable inputs. This input data is latched on the rising edge of $\overline{WR}$.

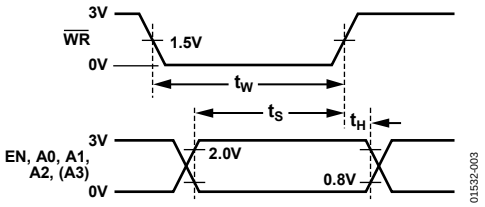


Figure 13. Timing Sequence

Figure 14 shows the reset pulse width, t_{RS}, and reset turn-off time, t_{OFF} ($\overline{RS}$).

Note that all digital input signal rise and fall times are measured from 10% to 90% of 3 V, $t_R = t_F = 20$ ns.

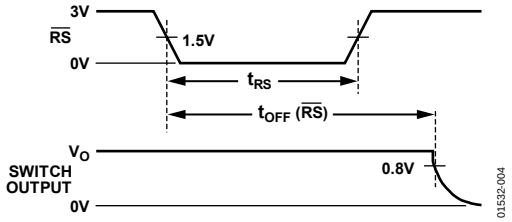


Figure 14. Reset Pulse

TEST CIRCUITS

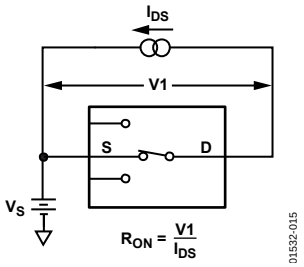


Figure 15. R_{ON}

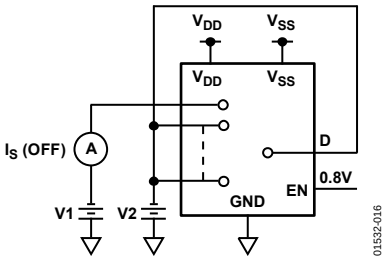


Figure 16. I_S (Off)

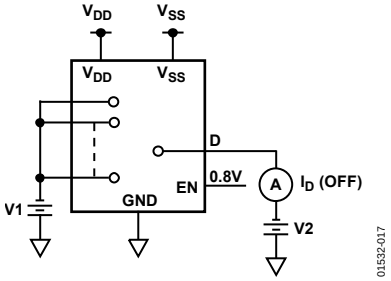


Figure 17. I_D (Off)

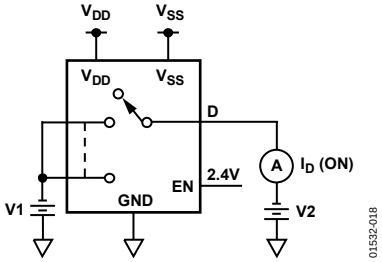


Figure 18. I_D (On)

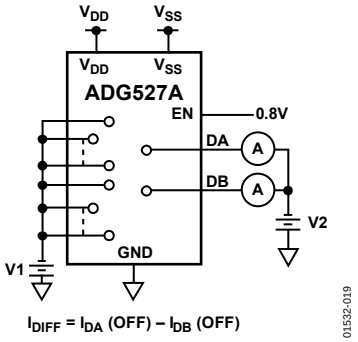


Figure 19. I_{DIFF}

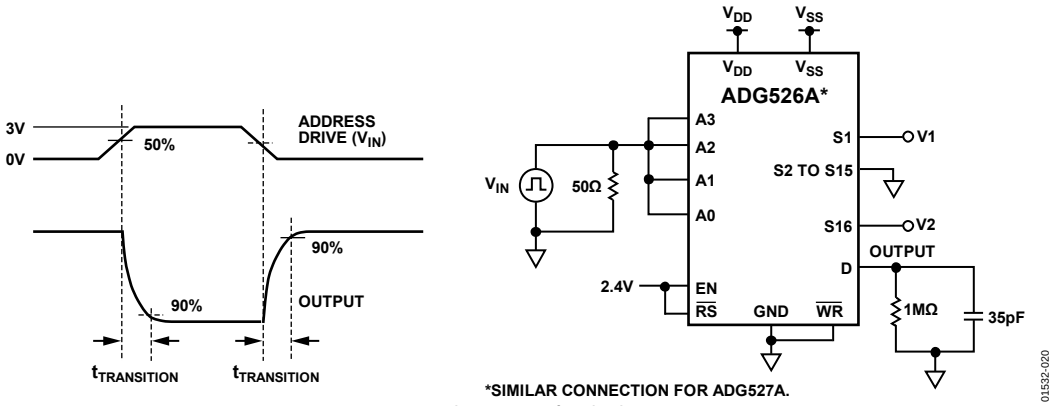


Figure 20. Switching Time of Multiplexer, $t_{TRANSITION}$

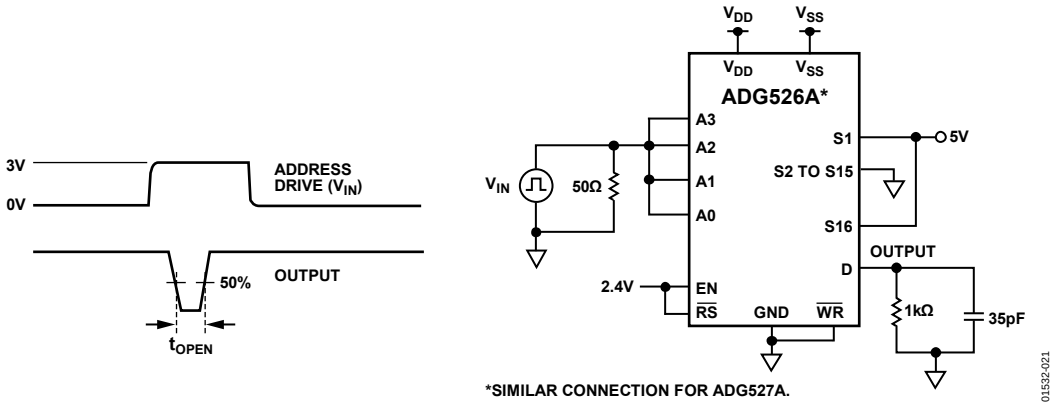


Figure 21. Break-Before-Make Delay, t_{OPEN}

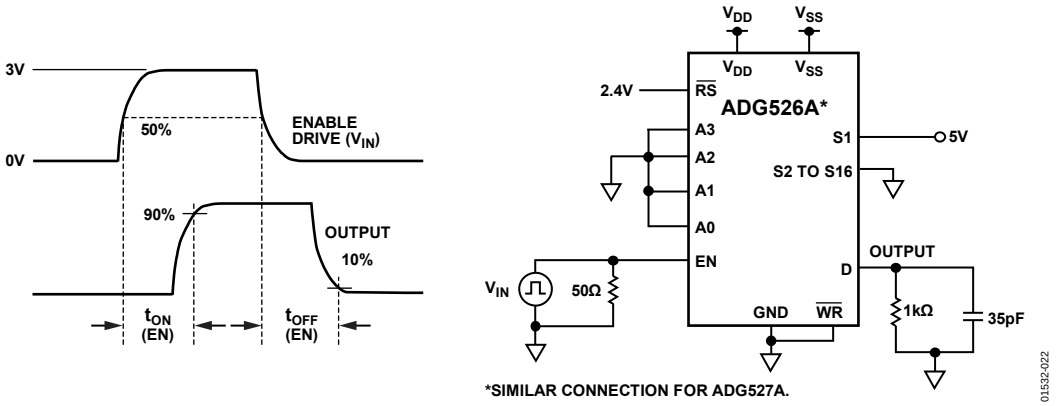


Figure 22. Enable Delay, t_{ON} (EN) t_{OFF} (EN)

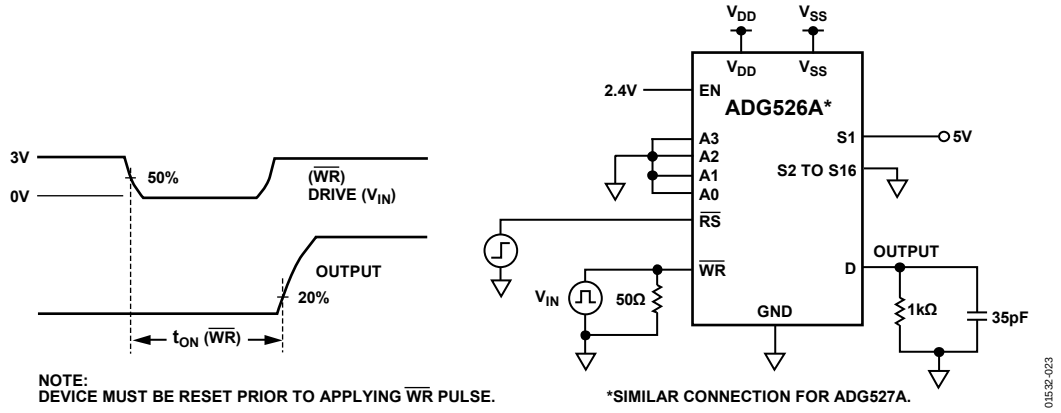


Figure 23. Write Turn-On Time, t_{ON} ($\overline{WR}$)

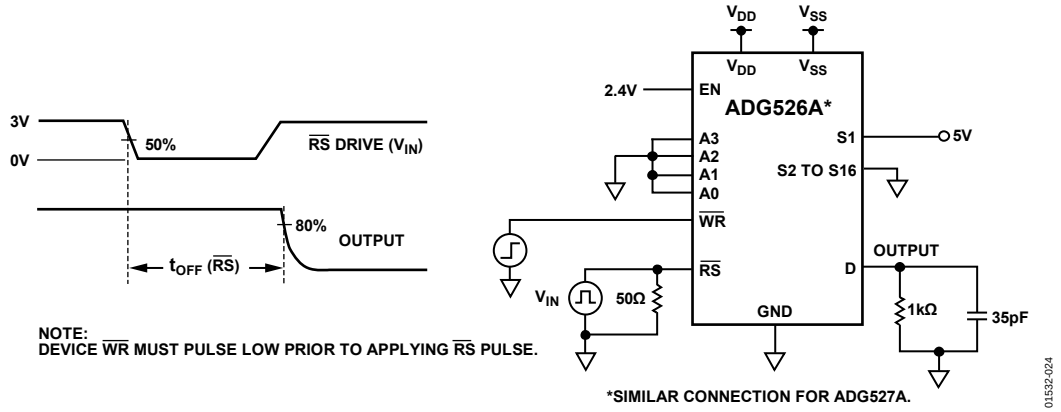


Figure 24. Reset Turn-Off, t_{OFF} ($\overline{RS}$)

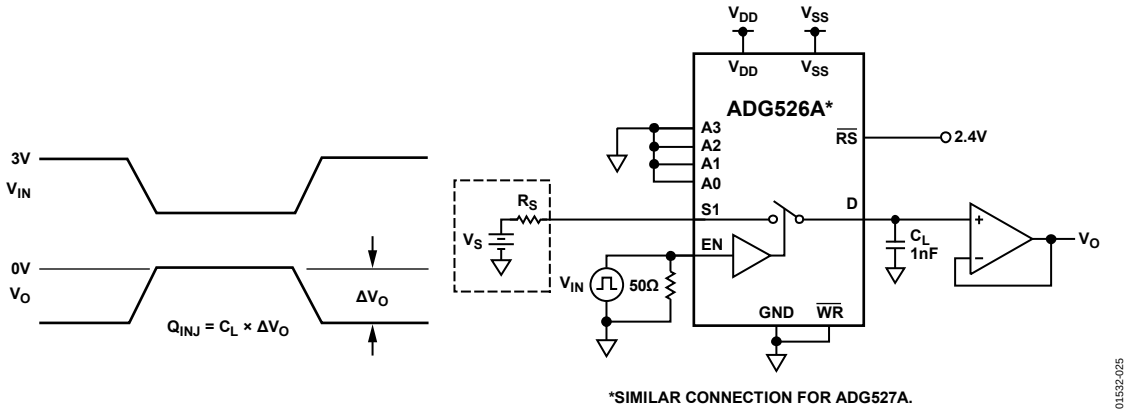
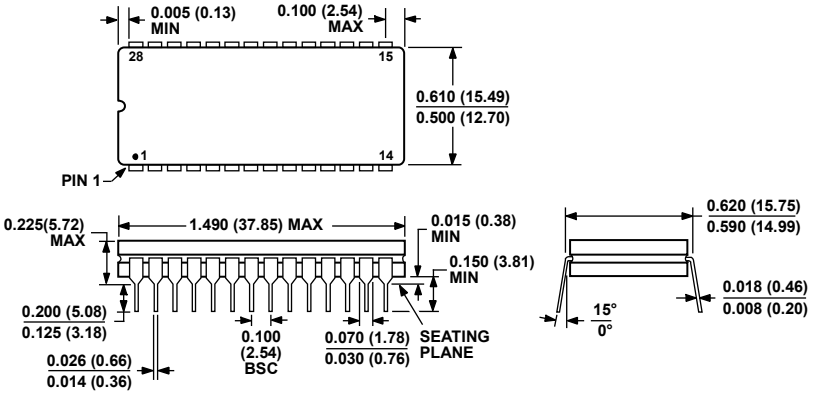


Figure 25. Charge Injection

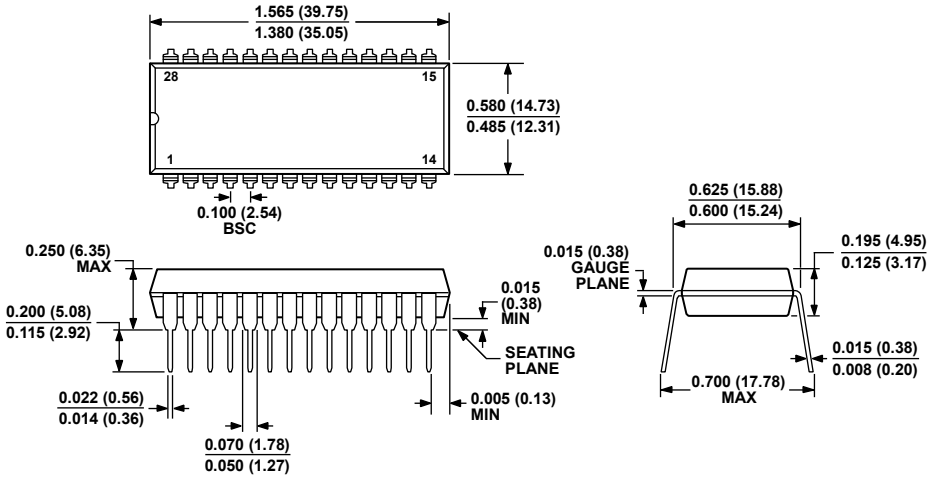
OUTLINE DIMENSIONS



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

030106-A

Figure 26. 28-Lead Ceramic Dual In-Line Package [CERDIP]
(Q-28)
Dimensions shown in inches and (millimeters)

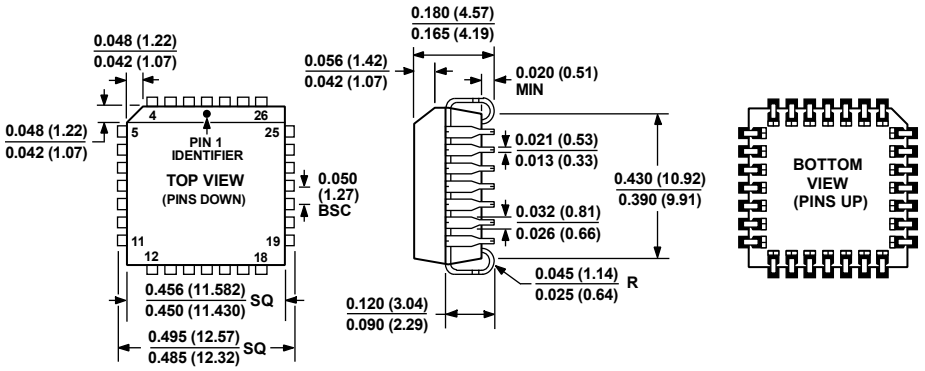


COMPLIANT TO JEDEC STANDARDS MS-011

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE LEADS.

071006-A

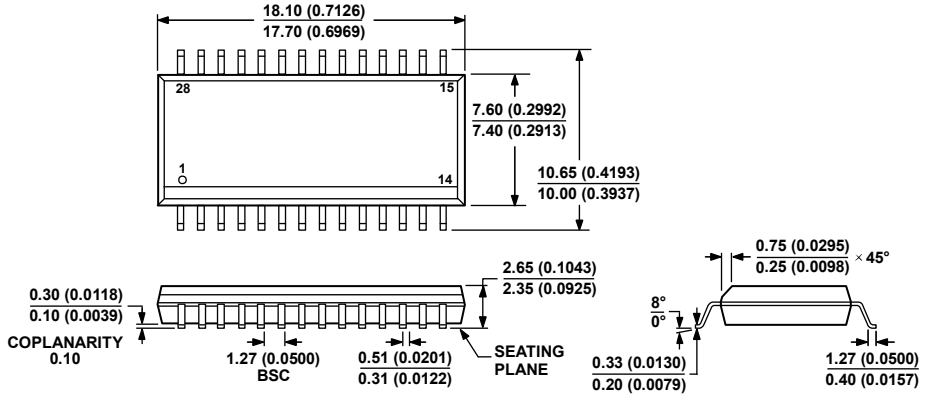
Figure 27. 28-Lead Plastic Dual In-Line Package [PDIP]
(N-28)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MO-047-AB
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

042508-A

Figure 28. 28-Lead Plastic Leaded Chip Carrier [PLCC]
(P-28A)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-013-AE
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060706-A

Figure 29. 28-Lead Standard Small Outline Package [SOIC] Wide Body
(RW-28)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG526AKN	−40°C to +85°C	28-Lead PDIP	N-28
ADG526AKNZ[1]	−40°C to +85°C	28-Lead PDIP	N-28
ADG526AKR	−40°C to +85°C	28-Lead SOIC	RW-28
ADG526AKR-REEL	−40°C to +85°C	28-Lead SOIC	RW-28
ADG526AKRZ[1]	−40°C to +85°C	28-Lead SOIC	RW-28
ADG526AKRZ-REEL[1]	−40°C to +85°C	28-Lead SOIC	RW-28
ADG526AKP	−40°C to +85°C	28-Lead PLCC	P-28A
ADG526AKP-REEL	−40°C to +85°C	28-Lead PLCC	P-28A
ADG526AKPZ[1]	−40°C to +85°C	28-Lead PLCC	P-28A
ADG526AKPZ-REEL[1]	−40°C to +85°C	28-Lead PLCC	P-28A
ADG526ATQ	−55°C to +125°C	28-Lead CERDIP	Q-28
ADG526ABQ	−40°C to +85°C	28-Lead CERDIP	Q-28
ADG526ATCHIPS			DIE
ADG527AKN	−40°C to +85°C	28-Lead PDIP	N-28
ADG527AKNZ[1]	−40°C to +85°C	28-Lead PDIP	N-28
ADG527AKR	−40°C to +85°C	28-Lead SOIC	RW-28
ADG527AKR-REEL	−40°C to +85°C	28-Lead SOIC	RW-28
ADG527AKRZ[1]	−40°C to +85°C	28-Lead SOIC	RW-28
ADG527AKP	−40°C to +85°C	28-Lead PLCC	P-28A
ADG527AKPZ[1]	−40°C to +85°C	28-Lead PLCC	P-28A

[1] Z = RoHS Compliant Part, # denotes RoHS complaint product, may be top or bottom marked.

NOTES

D01532-0-6/08(C)